WHAT IS CLAIMED

1. A method for processing a plurality of instruction threads comprising:

retrieving a first instruction from a first thread of instructions;

retrieving a second instruction from a second thread of instructions;

executing the first instruction in a first stage of a processing pipeline; and

forwarding the first instruction to a next stage of the processing while forwarding the second instruction to the first stage of the processing pipeline such that the first instruction and the second instruction can be executed simultaneously in the processing pipeline.

2. The method for processing a plurality of instruction threads according to claim 1, further comprising:

transferring data from an input buffer to a packet task manager;

dispatching the data from the packet task manager to an analysis machine;

classifying the data in the analysis machine; and

modifying and forwarding the data in a packet manipulator.

3. The method for processing a plurality of instruction threads according to claim 1, further comprising transferring the data after modifying and forwarding to an output buffer.

4. The method for processing a plurality of instruction threads according to claim 1, further comprising processing data at a rate of at least 10 Gbs.

5. An apparatus for processing a plurality of instruction threads, said apparatus comprising:

a processing pipeline including a plurality of stages coupled to receive and process the plurality of instruction threads such that, during a processing period, each of the plurality of stages of the processing pipeline is operating on a different one of the instruction threads from the plurality of instruction threads.

6. The apparatus according to claim 5, further comprising;

an analysis machine having multiple pipelines, wherein one pipeline is dedicated to directly manipulating individual data bits of a bit field;

a packet task manager operationally connected to said analysis machine; and,

a packet manipulator operationally connected to said analysis machine.

7. The apparatus according to claim 6, wherein said analysis machine is multi-threaded.

8. The apparatus according to claim 6, wherein said analysis machine has 32 threads.

9. The apparatus according to claim 6, further comprising:

a packet task manager operationally connected to said analysis machine;

a packet manipulator operationally connected to said analysis machine; and

a global access bus including a master request bus and a slave request bus separated from each other and pipelined.

10. The apparatus according to claim 6, further comprising:

an external memory engine operationally connected to said analysis machine; and

a hash engine operationally connected to said analysis machine.

11. The apparatus according to claim 9, further comprising:

packet input global access bus software code used for flow of data packet information from a flexible input data buffer to an analysis machine.

12. The apparatus according to claim 9, further comprising:

packet data global access bus software code used for flow of packet data between a flexible data input bus and a packet manipulator.

13. The apparatus according to claim 9, further comprising:

statistics data global access bus software code used for connection of an analysis machine to a packet manipulator.

14. The apparatus according to claim 9, further comprising:

private data global access bus software code used for connection of an analysis machine to an internal memory engine submodule.

15. The apparatus according to claim 9, further comprising:

lookup global access bus software code used for connection of an analysis machine to an internal memory engine submodule.

16. The apparatus according to claim 9, further comprising:

results global access bus software code used for providing flexible access to an external memory.

17. The apparatus according to claim 9, further comprising:

results global access bus software code used for providing flexible access to an external memory.

18. The apparatus according to claim 9, further comprising:

a bi-directional access port operationally connected to said analysis machine;

an input buffer operationally connected to said analysis machine; and

an output buffer operationally connected to said analysis machine.